**CDA 4213L 001/CIS 6930 012**

**Fall 2019**

**CMOS VLSI Design**

Lab 1 Report

Canvas Submission

Due: 11:59 PM, 15th Sept. 2019

Note: Upload PDF version of this report. Only PDF format is accepted.

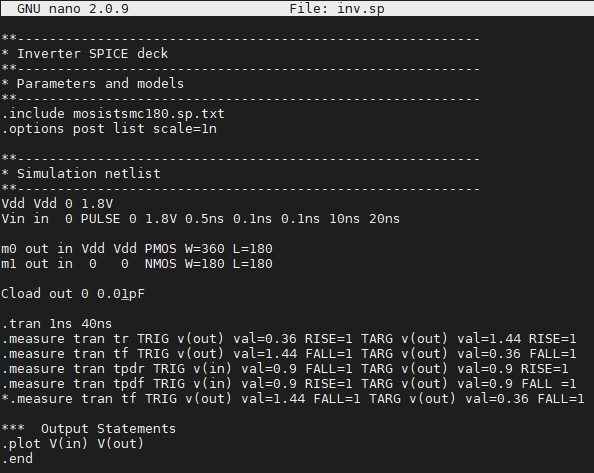
|  |  |
| --- | --- |
| Today’s Date: | 9/4 |
| Your Name: | Boyang Wu |
| Your U Number: | U95035892 |
| No. of Hours Spent: | 4 hours |
| Exercise Difficulty: (Easy, Average, Hard) | Average |
| Any Other Feedback: | Needs better documentation |

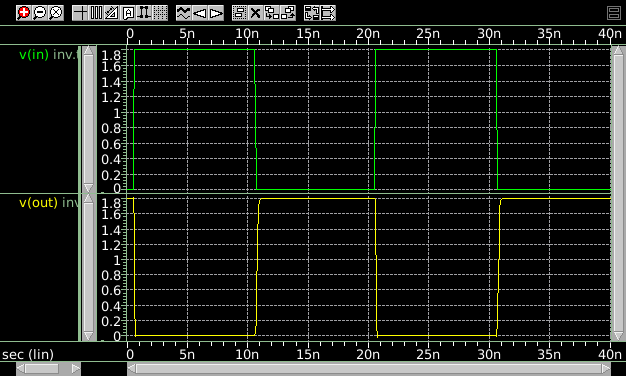
**Question 1: Inverter**

1. Complete the following table with values estimated in your simulations

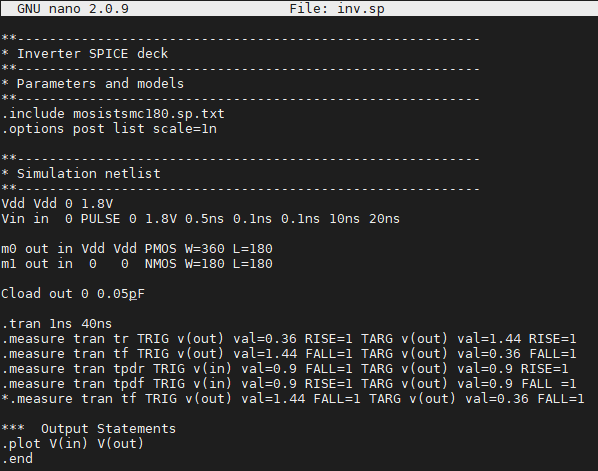
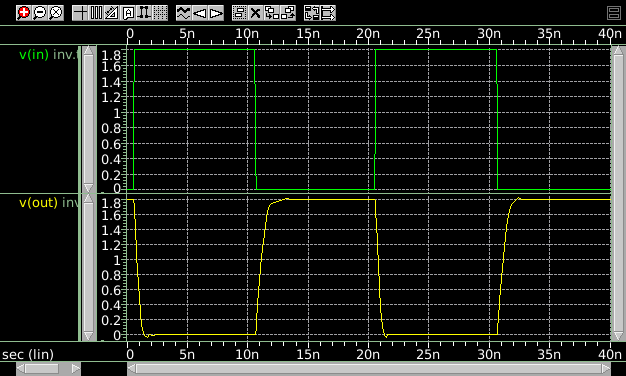
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Cload** | **tr** | **tf** | **tpdr** | **tpdf** |
| 0.01 pF | 1.261e-10 | 7.594e-11 | 1.097e-10 | 7.506e-11 |
| 0.05pF | 6.196e-10 | 4.282e-10 | 4.395e-10 | 3.113e-10 |
| 0.1pF | 1.238e-09 | 7.968e-10 | 8.952e-10 | 5.651e-10 |

1. For each Cload, show your hspice netlist (.sp file contents) and the waveform results. Use as many pages as needed.

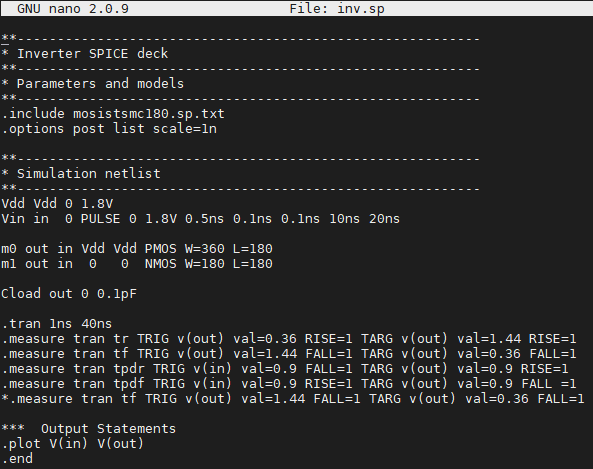
**0.01pF**

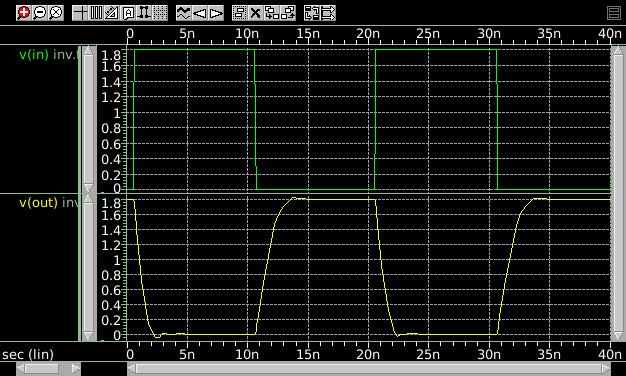


**0.05pF**



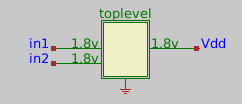
**0.1pF**

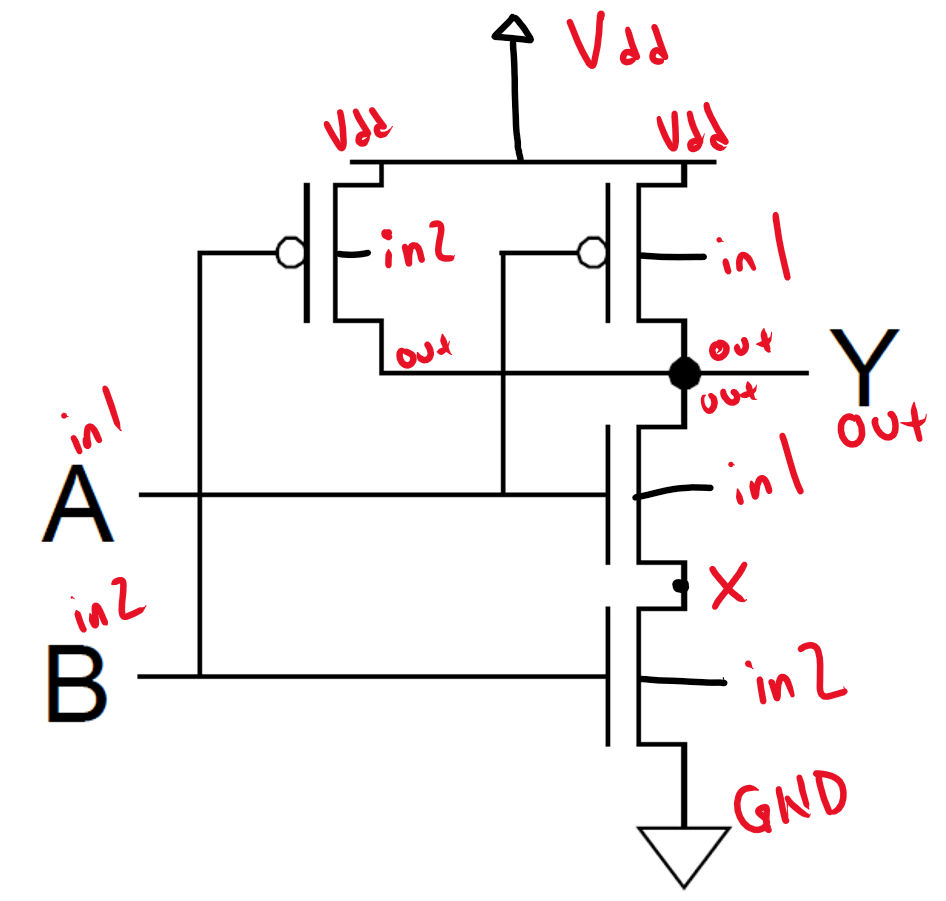




**Question 2: 2-input NAND Gate**

1. Transistor level diagram





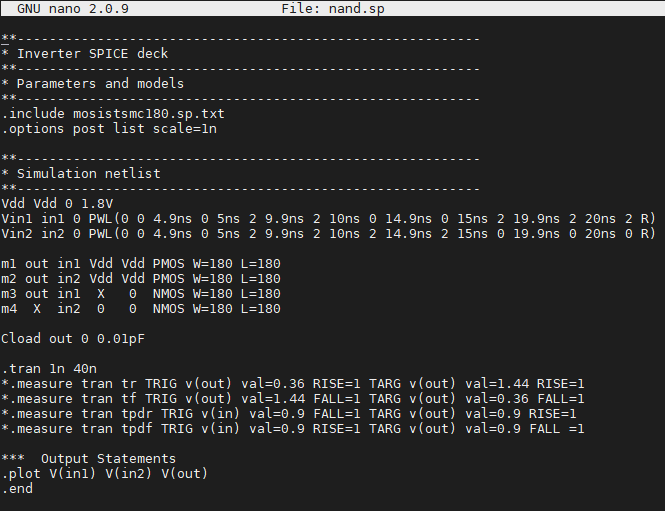
1. Spice netlist (.sp file contents)

**0-5ns is input 00**

**5ns-10ns is input 11**

**10ns-15ns is input 01**

**15ns-20ns is input 10**



1. Waveform results (show waveforms for all possible input combinations)

**0-5ns is input 00**

**5ns-10ns is input 11**

**10ns-15ns is input 01**

**15ns-20ns is input 10**

**The tiny spikes at 15ns and 20ns are due to the 0.1ns of inputs switching**

